CLAIMS

Please amend the claims and add new claims as shown in the following claim listing.

1. (Currently amended) A logic circuit comprising:

~~a~~ control flow logic to select and fetch a trace descriptor for processing, the fetched trace descriptor including at least one dependency descriptor, ~~the~~ a dependency descriptor including dependency information for an instruction sequence and ~~a location~~ an address of the instruction sequence; and

~~a~~ data flow logic coupled to the control flow logic to execute the instruction sequence according to the dependency information in the dependency descriptor.

2. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the control flow logic and the data flow logic, the storage area to store the dependency descriptor from the fetched trace descriptor by the control flow logic.

3. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the control flow logic, the storage area to store trace descriptors.

4. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the data flow logic, the storage area to store instructions contiguously based on dependency information.

5. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the data flow logic and control flow logic, the storage area to store live-out data.

6. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the control flow logic, the storage area to map live-in and live-out data.

7. (Canceled).

8. (Previously presented) The logic circuit of claim 1 wherein the trace descriptor includes aggregate live-in data for a plurality of dependency descriptors in the trace descriptor.

9. (Previously presented) The logic circuit of claim 1 wherein the trace descriptor includes aggregate live-out data for a plurality of dependency descriptors in the trace descriptor.

10. (Currently amended) A computer system comprising:

at least one memory device to store trace descriptors and instruction sequences;

a bus coupled to the at least one memory device;

~~a~~ control flow logic ~~device~~ to select and fetch one of the trace descriptors, the fetched trace descriptor including a plurality of dependency descriptors having ~~location~~ locations of corresponding instruction sequences and having dependency information for corresponding instruction sequences; and

~~a~~ data flow logic ~~device~~ coupled to the control flow logic ~~device~~ to receive a dependency descriptor dispatched from the control flow logic ~~device~~, to fetch an instruction sequence corresponding to the received dependency descriptor, and to execute the fetched instruction sequence.

11. (Currently amended) The computer system of claim 10 comprising an issue window coupled between the control flow logic ~~device~~ and the data flow logic ~~device~~, the issue window to store the dependency descriptor dispatched from the control flow logic ~~device~~.

12. (Canceled).

13. (Previously presented) The computer system of claim 10 wherein the at least one memory unit is to store an instruction sequence contiguously based on dependency information.

14. (Currently amended) The computer system of claim 10 comprising a storage area coupled to the data flow logic ~~device~~ and control flow logic ~~device~~, the storage area to store live-out data.

15. (Previously presented) The computer system of claim 10 comprising a storage area coupled to the control flow logic, the storage area to map live-in and live-out data.

16. (Canceled).

17. (Previously presented) The computer system of claim 10 wherein the fetched trace descriptor includes aggregate live-in data for dependency descriptors in the fetched trace descriptor.

18. (Previously presented) The computer system of claim 10 wherein the fetched trace descriptor includes aggregate live-out data for dependency descriptors in the fetched trace descriptor.

19. (Currently amended) The computer system of claim 10 wherein dependency information of the received dependency descriptor includes live-in and live-out data.

20. (Currently amended) A method of processing instructions comprising:

selecting and fetching a trace descriptor in accordance with program control flow;

identifying from the fetched trace descriptor a dependency descriptor including dependency information for a set of instructions and ~~a location~~ an address of the set of instructions;

fetching the set of instructions ~~from the location~~ using the address in the dependency descriptor; and

executing the set of instructions according to the dependency information in the dependency descriptor.

21. (Previously presented) A method according to claim 20 comprising:

updating live-out data in a storage area.

22. (Currently amended) A method according to claim 20 comprising:

storing the identified dependency descriptor from ~~a~~ control flow logic into a storage area; and

reading the dependency descriptor out of the storage area into ~~a~~ data flow logic.

23. (Previously presented) A method according to claim 20 wherein the fetching of the set of instructions is completed just in time for execution.

24. (Previously presented) A method according to claim 20 wherein the executing comprises executing instructions out of order.

25. (Previously presented) A method according to claim 21 comprising:

updating the architectural state using data in the storage area.

26. (Previously presented) A method according to claim 25 comprising:

recovering an earlier architectural state after a misprediction using data in the storage area.

27. (Previously presented) A method according to claim 20 wherein the selecting comprises predicting a next trace descriptor to process.

28. (Currently amended) A machine-readable medium that provides instructions, which when executed by a machine cause the machine to perform operations comprising:

selecting and fetching a trace descriptor in accordance with program control flow;

identifying from the fetched trace descriptor a dependency descriptor including dependency information for a set of instructions and ~~a location~~ an address of the set of instructions;

~~storing the dependency descriptor in an issue window to await assignment to an execution unit;~~

fetching the set of instructions ~~from the location~~ using the address in the dependency descriptor; and

executing the set of instructions according to the dependency information in the dependency descriptor.

29. (Previously presented) The machine-readable medium of claim 28, wherein the operations comprise:

updating live-out data in a storage area.

30. (Currently amended) The machine-readable medium of claim 28, wherein the operations comprise:

storing the dependency descriptor in an issue window by control flow logic; and

reading the dependency descriptor out of the issue window into data flow logic.

31. (New) The logic circuit of claim 1 wherein the fetched trace descriptor includes a plurality of dependency descriptors having addresses of corresponding instruction sequences and having dependency information for corresponding instruction sequences.

32. (New) The logic circuit of claim 1 wherein the dependency information includes live-in data.

33. (New) The logic circuit of claim 1 wherein the dependency information includes live-out data.